forming the steps (S**10**) to (S**110**) above, MOSFET **1** is manufactured and the semiconductor device manufacturing method according to the present embodiment is completed. Thus, according to the semiconductor device manufacturing method in the present embodiment, MOSFET **1** as the semiconductor device according to the present embodiment above capable of fixing a potential at the surface portion of the semiconductor layer located outside the active region can be manufactured.

Second Embodiment

[0090] A semiconductor device and a semiconductor device manufacturing method according to a second embodiment of the present invention will now be described. Initially, a structure of a MOSFET **2** as the semiconductor device according to the present embodiment will be described with reference to FIGS. **16** to **19**. Here, FIG. **18** is a plan view showing a top surface of semiconductor substrate **10** provided in MOSFET **2**. In addition, FIG. **19** is a plan view showing a top surface of MOSFET **2**. Referring to FIGS. **16** and **17**, MOSFET **2** is basically the same in structure and effect as MOSFET **1** as the semiconductor device according to the first embodiment above. MOSFET **2**, however, is different from MOSFET **1** in connection between the potential fixing region and the source interconnection and connection between the gate electrode and the gate interconnection.

[0091] Referring to FIG. **19**, source interconnection **60** is arranged to lie over active region **10**B when viewed two-dimensionally and is electrically connected to source region **16** through source electrode **50**, as in the first embodiment. Here, in the present embodiment, source interconnection **60** includes a source interconnection extension portion **60**A serving as a first interconnection extension portion extending beyond outer peripheral trench **22** to potential fixing region **10**C and it is electrically connected to potential fixing region **10**C in source interconnection extension portion **60**A.

[0092] Gate interconnection **70** is arranged to lie over potential fixing region **10**C when viewed two-dimensionally, as in the first embodiment. Here, in the present embodiment, gate interconnection **70** includes a gate interconnection extension portion **70**A serving as a second interconnection extension portion extending beyond outer peripheral trench **22** to gate electrode **40** and it is electrically connected to gate electrode **40** in gate interconnection extension portion **70**A.

[0093] Then, a semiconductor device manufacturing method according to the present embodiment will be described with reference to FIGS. **5** and **16** to **29**. Here, FIGS. **20**, **22**, **24**, **26**, and **28** partially show a cross-sectional structure of MOSFET **2** along the line C-C in FIG. **19**, and FIGS. **21**, **23**, **25**, **27**, and **29** partially show a cross-sectional structure of MOSFET **2** along the line D-D in FIG. **19**. The semiconductor device manufacturing method according to the present embodiment is basically performed in the steps the same as those in the semiconductor device manufacturing method according to the first embodiment, and achieves the same effect. In addition, in the semiconductor device manufacturing method according to the present embodiment, MOSFET **2** as the semiconductor device according to the present embodiment above is manufactured.

[0094] Referring to FIG. **5**, initially, the semiconductor substrate preparation step is performed as the step (S**10**). Referring to FIGS. **20** and **21**, in this step (S**10**), as in the first embodiment, semiconductor substrate **10** including base substrate **11**, drift layer **12**, and body layer **13** is prepared.

[0095] Then, the trench formation step is performed as the step (S**20**). Referring to FIGS. **22** and **23**, in this step (S**20**), as in the first embodiment, trench **20** opening on the main surface **10**A side and penetrating body layer **13** to reach drift layer **12** is formed in semiconductor substrate **10**. In addition, referring to FIG. **18**, in this step (S**20**), outer peripheral trench **22** surrounding an outer periphery of a region where active region **10**B should be formed in the subsequent step (S**30**) and inner trench **21** which is trench **20** other than outer peripheral trench **22**, arranged in the region above where active region **10**B should be formed, are formed. Here, in the present embodiment, outer peripheral trench **22** is formed without extending toward the region where potential fixing region **10**C should be formed in the subsequent step (S**30**).

[0096] Then, the ion implantation step is performed as the step (S**30**). In this step (S**30**), as in the first embodiment, the electric field relaxing region formation step as the step (S**31**) and the contact region formation step as the step (S**32**) are performed.

[0097] Referring to FIGS. **24** and **25**, initially, in the step (S**31**), electric field relaxing region **17** extending to be in contact with outer peripheral trench **22** is formed in drift layer **12**. Then, in the step (S**32**), contact regions **14**, **15** and source region **16** are formed in the region including main surface **10**A. Thus, active region **10**B including contact region **14** and source region **16** and potential fixing region **10**C including contact region **15**, where body layer **13** is exposed, are formed (see FIG. **18**). Here, since outer peripheral trench **22** is formed without extending toward potential fixing region **10**C in the present embodiment, potential fixing region **10**C is formed without extending toward active region **10**B.

[0098] Then, the activation annealing step is performed as the step (S**40**). In this step (S**40**), as in the first embodiment, semiconductor substrate **10** is heated. Then, the oxide film formation step is performed as the step (S**50**). Referring to FIGS. **26** and **27**, in this step (S**50**), as in the first embodiment, gate oxide film **30** and protection oxide film **31** are formed across the region including the wall surface of trench **20** and main surface **10**A.

[0099] Then, the gate electrode formation step is performed as the step (S**60**). Referring to FIGS. **28** and **29**, in this step (S**60**), as in the first embodiment, gate electrode **40** in contact with gate oxide film **30** is formed. Here, in the present embodiment, since outer peripheral trench **22** is formed without extending toward potential fixing region **10**C, gate electrode **40** is formed without extending toward potential fixing region **10**C.

[0100] Then, the interlayer insulating film formation step is performed as the step (S**70**). In this step (S**70**), as in the first embodiment, interlayer insulating film **32** is formed to be in contact with gate electrode **40** and protection oxide film **31**.

[0101] Then, the ohmic electrode formation step is performed as the step (S**80**). Referring to FIGS. **16** and **17**, in this step (S**80**), as in the first embodiment, source electrode **50** and drain electrode **51** are formed.

[0102] Then, the source interconnection formation step is performed as the step (S**90**). In this step (S**90**), referring to FIGS. **16** to **19**, for example, with the vapor deposition method, source interconnection **60** composed of Al which is a conductor is formed to lie over active region **10**B. Then, in the present embodiment, source interconnection **60** is formed to include source interconnection extension portion **60**A extending beyond outer peripheral trench **22** to potential fixing region **10**C.